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□ -10V□+10VDC□□□□□□□□□□□□□□□
□ □□CPU□□□□M4801□M4802□□□□□□□□□□□□□□□□□□□□□□□□□□□
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DA□□□ M4800DA

DA	ANALOG DEVICES□□ AD5547
□□□	16bit(1LSB: 305µV)
□□□□	±1LSB(T=25°C□Vin=5.0V)
□□□□□□□□□□□	±2LSB(T=0-40°C□Vin=4.5-5.5V)
□□□□	150µsec(MAX)
□□□□□□□□	2ch
□□□□□□	±10V
□□□□□□	0□40°C
□□□□	DC+5V±0.5V
□□□□□	280mA(MAX)
□□□□□mm□	90W×90D×20H

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URL□http://homepage2.nifty.com/logicpack/

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CN1□CN2□□□L□MIL□□□□OMRON□□ XG4C-5034□	2□

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□□□□CPU□□□□□□□□□□□□□□□□□□M801□JP15□M802□JP20□□
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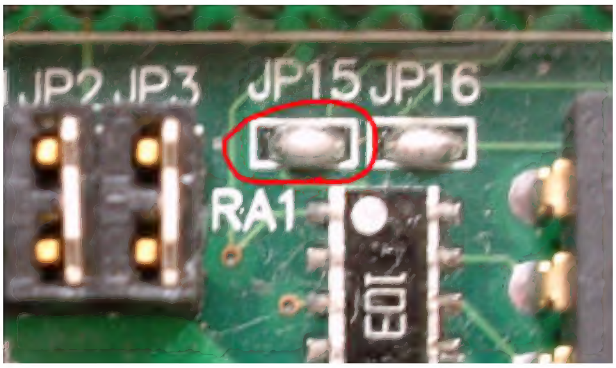
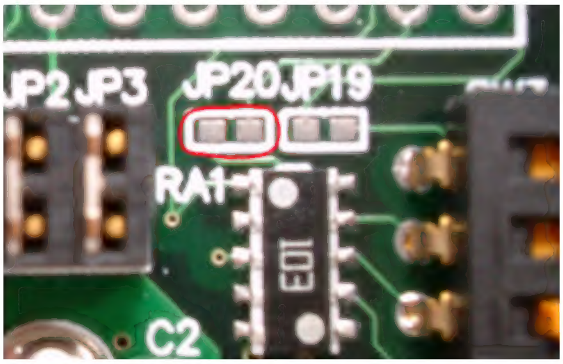
<M801>



<M802>



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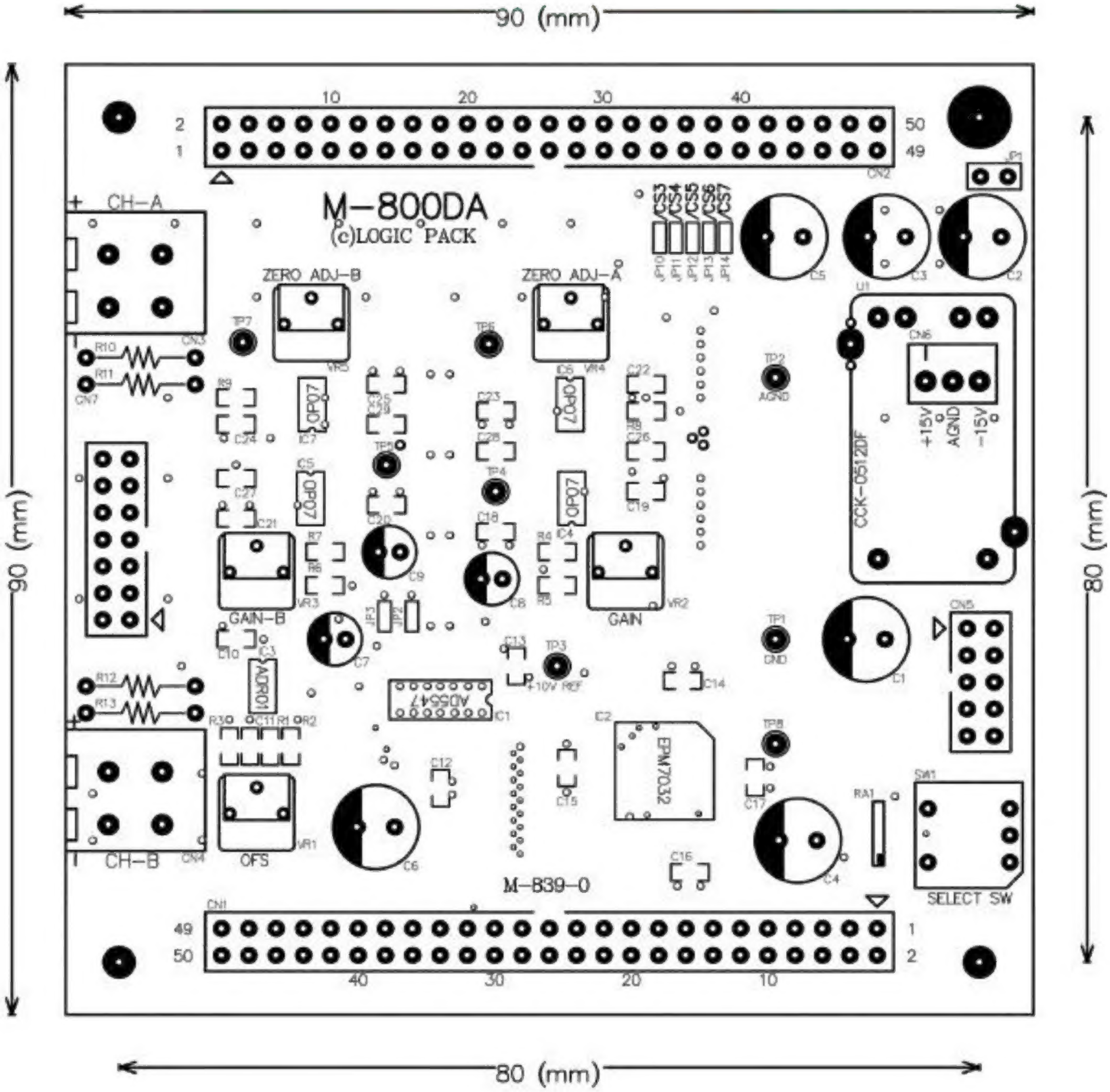

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CN1	MIL50	
50	VCC	
49	GND	
48	D0/P40	
47	D1/P41	
46	D2/P42	
45	D3/P43	
44	D4/P44	
43	D5/P45	
42	D6/P46	
41	P47/D7	
40	P30/D8	
39	P31/D9	
38	P32/D10	
37	P33/D11	
36	P34/D12	
35	P35/D13	
34	P36/D14	
33	P37/D15	
32	P10/A0	
31	P11/A1	
30	P12/A2	
29	P13/A3	
28	P14/A4	
27	P15/A5	CPU
26	P16/A6	
25	P17/A7	
24	P20/A8	
23	P21/A9	
22	P22/A10	
21	P23/A11	
20	P24/A12	
19	P25/A13	
18	P26/A14	
17	P27/A15	
16	P50/A16	
15	P51/A17	
14	P52/A18	
13	P53/A19	
12	P60/*WAIT	
11	P61/*BREQ	
10	P62/*BACK	
9	P63/*AS	
8	P64/*RD	
7	P65/*HWR	
6	P66/*LWR	
5	P67/CLK	
4	VCC	
3	VCC	
2	GND	
1	GND	

CN2	MIL50	
50	NMI	CPU
49	*STBY	
48	*ERSTI	
47	*ERSTO	
46	VCC	
45	VCC	
44	GND	
43	GND	
42	AVSS	
41	AVSS	
40	AVCC	
39	AVCC	
38	VREF	
37	VREF	
36	AN0/P70	
35	AN1/P71	
34	AN2/P72	
33	AN3/P73	
32	AN4/P74	
31	AN5/P75	
30	DA0/AN6/P76	
29	DA1/AN7/P77	
28	*RFSH/*IRQ0/P80	
27	*CS3/*IRQ1/P81	
26	*CS2/*IRQ2/P82	
25	ADTRG/*CS1/*IRQ3/P83	
24	*CS0/P84	
23	*TEND0/TCLKA/TP0/PA0	CPU
22	*TEND1/TCLKB/TP1/PA1	
21	TCLKC/TIOCA0/TP2/PA2	
20	TCLKD/TIOCB0/TP3/PA3	
19	A23/TIOCA1/TP4/PA4	
18	A22/TIOCB1/TP5/PA5	
17	A21/TIOCA2/TP6/PA6	
16	A20/TIOCB2/TP7/PA7	
15	*CS7/TMO0/TP8/PB0	
14	*CS6/DREQ0/TMIO1/TMP9/PB1	
13	*CS5/TMO2/TP10/PB2	
12	*CS4/*DREQ1/TMIO3/TP11/PB3	
11	*UCAS/Tp12/PB4	
10	SCK2/*LCAS/TP13/PB5	
9	TXD2/TP14/PB6	
8	RXD2/TP15/PB7	
7	TXD0/P90	
6	RXD0/P92	
5	*IRQ4/SCK0/P94	
4	*IRQ5/SCK1/P95	
3	GND	
2	DSR	
1	DTR	

CN3	DA OUT CH-A ML-1400-S1L-2
+	Analog Output CH-A
-	Analog GND CH-A

CN4	DA OUT CH-B ML-1400-S1L-2
+	Analog Output CH-B
-	Analog GND CH-B

CN7	MIL14
1	Analog GND CH-B
2	Analog Output CH-B
3	NC
4	NC
5	-15V
6	-15V
7	AGND
8	AGND
9	+15V
10	+15V
11	NC
12	NC
13	Analog GND CH-A
14	Analog Output CH-A

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JP1 □□□

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JP10□ 11□ 12□ 13□ 14 /CS□□□

JP10	JP11	JP12	JP13	JP14	
□□□□	□□□□	□□□□	□□□□	□□□□	/CS3 *
□□□□	□□□□	□□□□	□□□□	□□□□	/CS4
□□□□	□□□□	□□□□	□□□□	□□□□	/CS5
□□□□	□□□□	□□□□	□□□□	□□□□	/CS6
□□□□	□□□□	□□□□	□□□□	□□□□	/CS7

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□□□ID□□□□SW1)

M-800DA□□□□□□□□□□□□□□□□ID□□□□□□□
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□□□ID□□□□□□□□□□SELECT SW□SW1□□□□□□□□
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I/O□□□□□□□

CPU□□□□□□□□□□□□□□□□□

□□□ID	CH-A Set Data	CH-B Set Data	CH-A+B Set Data	LDAC Output
0	+0000h	+0006h	+0004h	+0002h
1	+0100h	+0106h	+0104h	+0102h
2	+0200h	+0206h	+0204h	+0202h
3	+0300h	+0306h	+0304h	+0302h
4	+0400h	+0406h	+0404h	+0402h
5	+0500h	+0506h	+0504h	+0502h
6	+0600h	+0606h	+0604h	+0602h
7	+0700h	+0706h	+0704h	+0702h
8	+0800h	+0806h	+0804h	+0802h
9	+0900h	+0906h	+0904h	+0902h
A	+0a00h	+0a06h	+0a04h	+0a02h
B	+0b00h	+0b06h	+0b04h	+0b02h
C	+0c00h	+0c06h	+0c04h	+0c02h
D	+0d00h	+0d06h	+0d04h	+0d02h
E	+0e00h	+0e06h	+0e04h	+0e02h
F	+0f00h	+0f06h	+0f04h	+0f02h

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```
#define CS3_ADDR 0x600000                        /* /CS3 = 0x600000 */
#define CS4_ADDR 0x800000                        /* /CS4 = 0x800000 */
#define CS5_ADDR 0xA00000                        /* /CS5 = 0xA00000 */
#define CS6_ADDR 0xC00000                        /* /CS6 = 0xC00000 */
#define CS7_ADDR 0xE00000                        /* /CS4 = 0xE00000 */
#define OFS_ADDR CS3_ADDR

/* □□□ID□6 */
(*(volatile word *)(OFS_ADDR + 0x0600)) = 0x8000;    /* CH-A□8000□□□□ */
(*(volatile word *)(OFS_ADDR + 0x0602)) = 0;         /* LDAC */
```

[illegible]

[illegible]
[illegible]

[illegible]

[illegible]VR1 [illegible]

DA[illegible]0000h[illegible]CH-A[illegible]-10.000V±0.5mV[illegible]VR1[illegible]OFS[illegible]
[illegible]

[illegible]VR2 [illegible]

DA[illegible]FFFFh[illegible]CH-A[illegible]10.000V±0.5mV[illegible]VR2[illegible]GAIN[illegible]
[illegible]

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[illegible]

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[illegible] 2005[illegible]10[illegible]17[illegible]

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[illegible]438-0078 [illegible]1803-1
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E-mail logic_pack@nifty.com